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A DC-Coupled 50 Gb/s 0.064 pJ/bit Thin-Oxide Level Shifter in 28 nm FDSOI CMOS

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Abstract: High-speed optical interconnects require compact, low-power driver electronics for optical modulators. Inverter based CMOS driver circuits show very low power consumption. However, the output swing is typically limited to the supply voltage which is typically insufficient for optical modulators, requiring a cascoded output driver and level shifter. In this work, we present a new DC-coupled thin-oxide level shifter topology in a 28 nm FDSOI CMOS technology enabling data rates up to 50 Gb/s with a power efficiency of 0.064 pJ/bit.

Keywords: Level shifter, FDSOI CMOS, 28 nm

Classification: Integrated circuits (Analog)

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1 Introduction

The need for faster optical interconnects is identified by the roadmaps of multiple standard bodies such as the Ethernet alliance, the Optical Internetworking Forum (OIF) and Infiniband. Together with the increasing data rates, comes the challenge to increase the power efficiency and the integration density. Recently CMOS-based transceivers have shown bit rates exceeding 40 Gb/s at 2 pJ/bit or less [1, 2, 3]. To realize this low power consumption, high speed CMOS transceivers rely on multi-stage inverter based topologies. However, an inverter is most efficient when it is fully switching. As a result, the output voltage is limited to the supply voltage (V_{dd}), around 1 V for today's CMOS technologies. Lowering the supply voltage slows down the inverter stage, while increasing it can cause reliability issues. The latter is the largest problem as typical optical modulators, e.g. electro absorption modulators (EAM) or microring modulators, often require much higher voltage swings (2-3 V peak-to-peak) to have a sufficiently high extinction ratio (ER) [4, 5]. To generate a driving voltage that is larger than 1 V with inverter based driver circuits, a cascoded inverter driver (Fig. 1) [2, 6, 7] or a pseudo differential output driver [8, 9] can be used.

Cascoded inverter based drivers are favoured over pseudo differential inverter drivers because they provide a more effective way of biasing the modulator by an extra DC voltage, albeit at the cost of added complexity, since this topology requires an extra level shifted input (between V_{dd} and $2V_{dd}$) to drive the upper transistor. Generating this level shifted signal proves to be difficult for high speed applications. To obtain the required bandwidth an AC coupled level shifter [2, 6, 10] is frequently implemented, but can introduce bit errors when sending bit streams with a long sequence section of consecutive identical bits if not sized properly or working at a lower rate than designed for. DC-coupled level shifters [7, 11] do not have this problem and hence work for multi-rate applications, but are typically limited in maximum

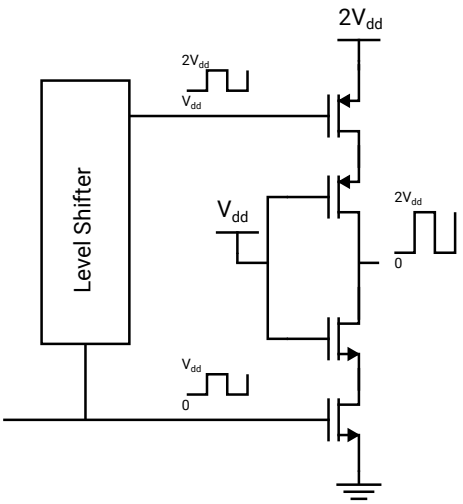


Fig. 1. A cascoded inverter driver with level shifter

speed. This work presents a high speed DC-coupled thin-oxide transistors-only level shifter in a 28 nm fully depleted silicon on insulator (FDSOI) technology that enables data rates up to 50 Gb/s. Thin-oxide transistors have the benefit that they are small and have less parasitic capacitance, but their break down voltage is much lower. Section 2 describes the changes made to the conventional level shifter to achieve the required speed. Section 3 continues with the high speed measurement results and a conclusion is formulated in Section 4.

2 The level shifter circuit

The proposed level shifter circuit (Fig. 3) is an improvement of a conventional level shifter (Fig. 2)[11]. The conventional level shifter uses only thin-oxide transistors to generate a DC shifted output signal. The nominal maximum drain-source voltage of the thin-oxide transistors is V_{dd}, while generating a signal between V_{dd} and $2V_{dd}$. Care has to be taken to not overdrive and break the thin-oxide transistors.

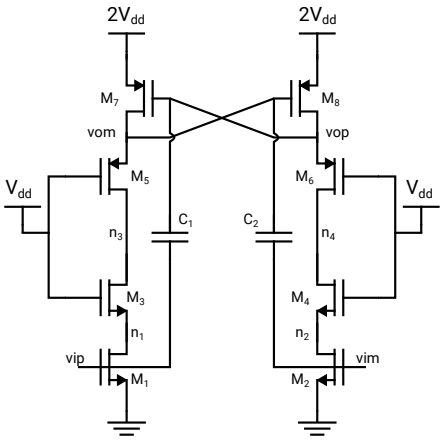


Fig. 2. A conventional level shifter circuit

In the conventional level shifter, when the positive input *vip* is pulled low (and negative input *vim* high), M_1 turns off and node n_1 is charged to V_{dd} trough M_3. Simultaneously M_2 turns on and pulls n_2 to 0 V. If no differential or pseudo differential signal is available, *vim* can be generated by inverting the signal *vip*. Node n_3 charges to $2V_{dd}$ and n_4 is pulled to *gnd*. Capacitors C_1 and C_2 boost the high frequency switching of *vop* and *vom* and increase the speed of the level shifter. A maximum bit rate of 16 Gb/s was found for the conventional level shifter in simulation for the used 28 nm FDSOI technology without a large area occupation. Increasing the operating speed of the level shifter requires some modifications and the proposed level shifter circuit is shown in Fig. 3.

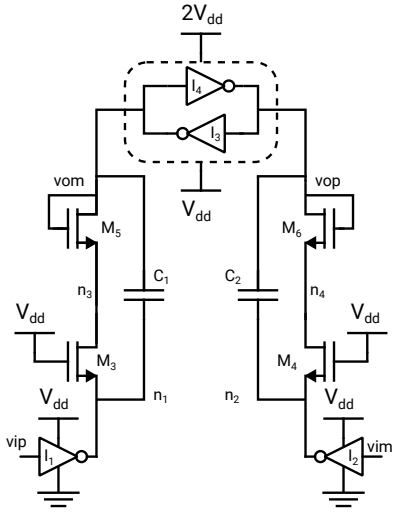


Fig. 3. The proposed high speed level shifter circuit

In the conventional level shifter, n_1 and n_2 are charged to V_{dd} by M_3 and M_4. During the charging process, the source impedance of M_3 and M_4 increases, which slows down the circuit dramatically. To increase the speed, we added in the proposed level shifter a PMOS device at node n_1 and n_2 to pull the nodes to V_{dd} when needed. The result is that nodes n_1 and n_2 are now driven by an inverter instead of a single NMOS device. This inverter has to be sized to drive both the capacitive voltage divider of C_1 with the load capacitance and the transistor M_3. Moving C_1 and C_2 behind the inverters I_1 and I_2 relaxes the circuit that drives the level shifter. The switching of output nodes *vom* and *vop* is faster by replacing M_7 and M_8 by the inverters I_3 and I_4. We replaced the cascode PMOS devices M_5 and M_6 by diode connected NMOS transistors to improve the startup behavior of the level shifter. Because of the diode connection, there is a very small static current (in the order of μA and limited by properly sizing M_3, M_4, M_5 and M_6) flowing when the transistor is conducting (n_1 or n_2 pulled to 0). However the added power consumption is negligible with respect to the total power consumption.

The nodes n_1 and n_2 are charged and discharged by inverters I_1 and

I_2, hence, M_3, M_4 can be made smaller. M_3 and M_4 are only needed to provide a low frequency path after the capacitors C_1 and C_2 boosted the data edges until the inverters I_3 and I_4 take over. Making M_3 and M_4 smaller further improves the high speed characteristics of the level shifter. Simulated waveforms of the nodes *vop*, n_4 and n_2 are shown in Fig 4.

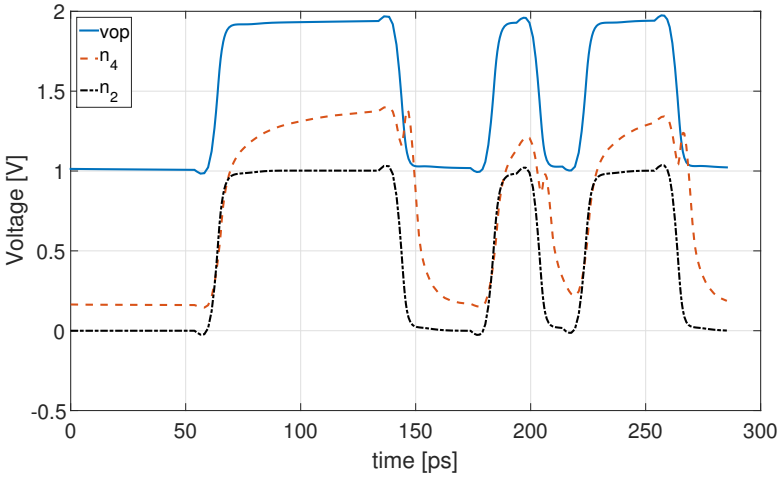


Fig. 4. Simulation results of the proposed level shifter with a 50 Gb/s input signal

An overall speed gain of a factor of 3 (16 Gb/s for the conventional level shifter and 50 Gb/s for the proposed level shifter) was found in simulation for the same transistor area. To reach 50 Gb/s with the conventional level shifter, M_3, M_4, M_5, M_6 need to be 50 times larger compared to the proposed level shifter, leading to a much larger area occupation. Thanks to the area reduction in the proposed level shifter, the power consumption decreases since lower parasitic capacitances need to be charged. The power efficiency drops from 0.08 pJ/bit (at 50 Gb/s) for the conventional level shifter to 0.06 pJ/bit (at 50 Gb/s) for the proposed level shifter. The power consumption of the stage driving the level shifter was not taken into account, but the drive strength of this stage can be lower for the proposed level shifter, making the power consumption gap between the proposed and the conventional level shifter more pronounced.

3 Measurements

The proposed level shifter circuit from Fig. 3 has been implemented in a 28 nm FDSOI CMOS technology. To be able to characterize the proposed level shifter in a 50 Ω environment, minimal input matching and an output buffer preserving the level shifting characteristic have been added as can be seen in Fig. 5. The input matching and output buffer are not needed when the level shifter is embedded inside a larger circuit and are only added to allow proper high speed testing. The input matching consists of a 100 Ω matching resistor between the inputs of inverters I_1 and I_2. To further increase the

matching of the input matching circuit, series inductors at the input are added. We assumed good matching when the reflection is below -10 dB. The output buffer is an inverter between $2\,V_{dd}$ and V_{dd}. This output buffer inverter serves as a realistic capacitive load to the level shifter as would be the case when using the level shifter in a complete modulator driver chip. When loading an inverter with high speed measurement equipment, with $50\,\Omega$ to ground, the inverter delivers DC current to that load and the output bits are distorted and show heavy duty cycle distortion. This ultimately leads to lower output bandwidth of the inverter output buffer. The problem with the DC current flowing into the measurement equipment is solved by using a DC block between the inverter and the measurement equipment. However, when using a DC block, the DC level of the shifted signals is lost. By placing a bias tee at the output we can simultaneously measure the AC and DC signals for the level shifter, as shown in Fig. 5. We used a high speed pattern generator to generate the pseudo random bit sequence (PRBS) signal and a 50 GHz sampling oscilloscope to capture the resulting eye diagrams.

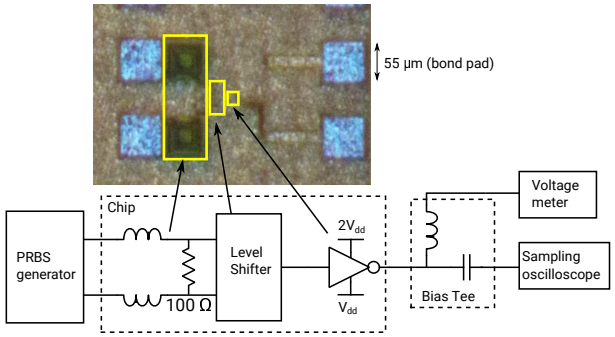
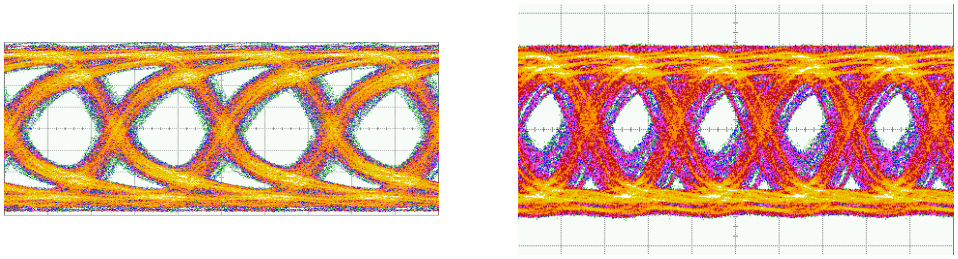


Fig. 5. Measurement setup containing a pattern generator for PRBS generation, a bias tee to measure the output DC voltage and a sampling oscilloscope to capture the eye diagrams

When an inverter based circuit is supplied with a random bitstream and the output is fully switching between 0 and V_{dd}, the average voltage at the output of the inverter will be $\frac{V_{dd}}{2}$. The measured DC voltage at the DC port of the bias tee is $\frac{3V_{dd}}{2}$ indicating that the output signal is correctly switching between V_{dd} and $2V_{dd}$. Fig. 6 shows the measurement results for 40 Gb/s and 50 Gb/s (PRBS $2^9 - 1$) with a nominal supply V_{dd} of 1 V. The eye diagrams are clearly open. Since we are measuring the output of an inverter with a $50\,\Omega$ oscilloscope, the measured amplitude is lower due to the voltage division from r_{on} of the transistors of the output inverter and the $50\,\Omega$ load. The level-shifting circuit, without in and output test circuits, consumes 3.2 mW (0.064 pJ/bit at 50 Gb/s): 2.8 mA from 1 V supply and 0.2 mA from the 2 V supply at 50Gb/s and measures only 0.002 mm^2.

Table I shows a comparison of this work with other reported CMOS level shifters for cascoded output inverter applications. The table combines AC and DC-coupled level shifters and shows that this work is competitive while



(a) (b)

Fig. 6. Measurement results for (a) 40 Gb/s (55 mV/div, 10 ps/div) and (b) 50 Gb/s (100 mV/div, 10 ps/div) with $V_{dd} = 1$ V

being DC-coupled. The power consumption information of the level shifters in the references are not seperately available since only the total driver power consumption is given.

Table I. Comparison of reported CMOS level shifters for cascoded output inverter applications

Reference	Technology	Bit rate	DC-coupled
[2]	28 nm SOI	60 Gb/s	no
[6]	65 nm	25 Gb/s	no
[7]	65 nm	18 Gb/s	yes
[10]	45 nm SOI	14 Gb/s	no
[11]	130 nm	1 Gb/s	yes
This work	28 nm SOI	50 Gb/s	yes

4 Conclusion

We presented improvements to a conventional level shifter circuit to enable data rates up to 50 Gb/s in 28 nm CMOS FDSOI. The level shifter consumes only 3.2 mW (0.064 pJ/bit at 50 Gb/s) while providing a DC-coupled level shifted signal between V_{dd} and $2V_{dd}$. The proposed changes also reduce the area and power consumption with respect to the conventional level shifter.

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